Machine Learning–Based Power Consumption Prediction for Logic Circuits

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Abstract: Due to growing circuit complexity and the need for energy-efficient operation, power con- sumption has emerged as a crucial design constraint for contemporary digital systems. Tra- ditional analytical and simulation-based power estimation methodologies often suffer from limited scalability and high computational cost when applied to large logic architectures. This research proposes a machine learning-based framework for predicting the dynamic power consumption of logic circuits using readily available circuit-level parameters.

A synthetic dataset is generated using logic-level power modeling by varying switching activity, load capacitance, supply voltage, operating frequency, and gate count. Supervised regression models including Linear Regression, Support Vector Regression, and Random For- est Regression are trained and evaluated using Mean Absolute Error, Root Mean Square Error, and coefficient of determination.

Unlike prior approaches that rely on post-layout or technology-dependent parameters, the proposed framework focuses on early-stage, technology-neutral power estimation. Experi- mental results demonstrate that ensemble learning significantly improves prediction accuracy while reducing estimation complexity. Although the study uses synthetic data, the frame- work provides a scalable foundation for early-stage power-aware logic circuit design and can be extended to real circuit benchmarks in future work..

Keywords: power consumption prediction, logic circuits, machine learning, energy-efficient computing, regression models, VLSI power estimation,

Introduction

Logic density, operating frequency, and system-level complexity have all significantly increased as a result of the ongoing scaling of digital integrated circuits. Consequently, power consumption has become a major design constraint that affects energy efficiency, thermal stability, and system dependability. The basic building blocks of all digital systems are logic circuits[1], and the longevity and general performance of contemporary electronic gadgets are directly impacted by their power dissipation. Strict power budgets need precise power prediction in early design phases in application areas such battery-powered embedded systems, Internet of Things (IoT) platforms, and portable electronics [2, 3].

In logic circuits, power consumption is often divided into two categories: static and dynamic. In switching-intensive designs, dynamic power dissipation predominates. Switching activity, load capacitance, supply voltage, operating frequency, and circuit size are some of the interconnected factors that affect dynamic power. The main causes of power dissipation in logic circuits are shown in Figure 1. Power-aware architectural choices and design optimization depend on accurate modeling of these variables.

Analytical and simulation-based methods are the two main categories into which conventional power estimating techniques fall. Simplified mathematical expressions resulting from capacitance assumptions and circuit switching behavior are the foundation of analytical models. Although these techniques are computationally inexpensive, they frequently fail to capture nonlinear interactions between circuit param- eters, which results in limited accuracy for complicated logic architectures [3]. Although simulation-based methods, like gate-level and transistor-level simulations, improve accuracy by simulating intricate circuit behavior, they are not appropriate for quick design space exploration due to their large computational overhead and lengthy execution times [4].

The trade-off between accuracy and processing cost in conventional power estimating methods is illus- trated in Figure 2. Alternative modeling approaches are required because simulation-based approaches become more and more unfeasible for early-stage design review as circuit complexity rises.

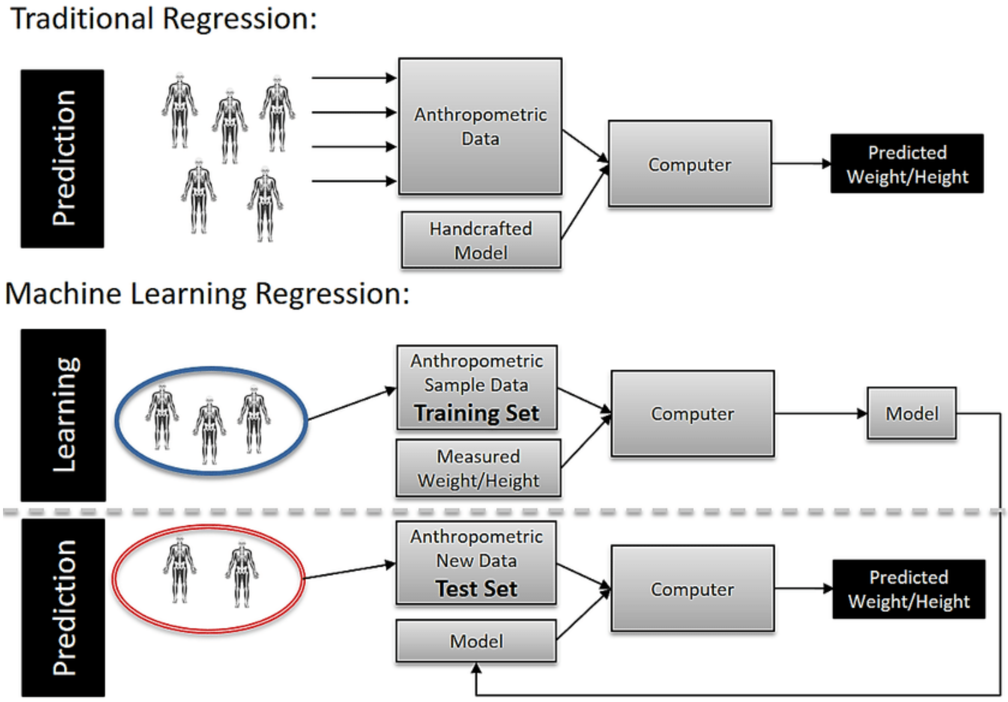
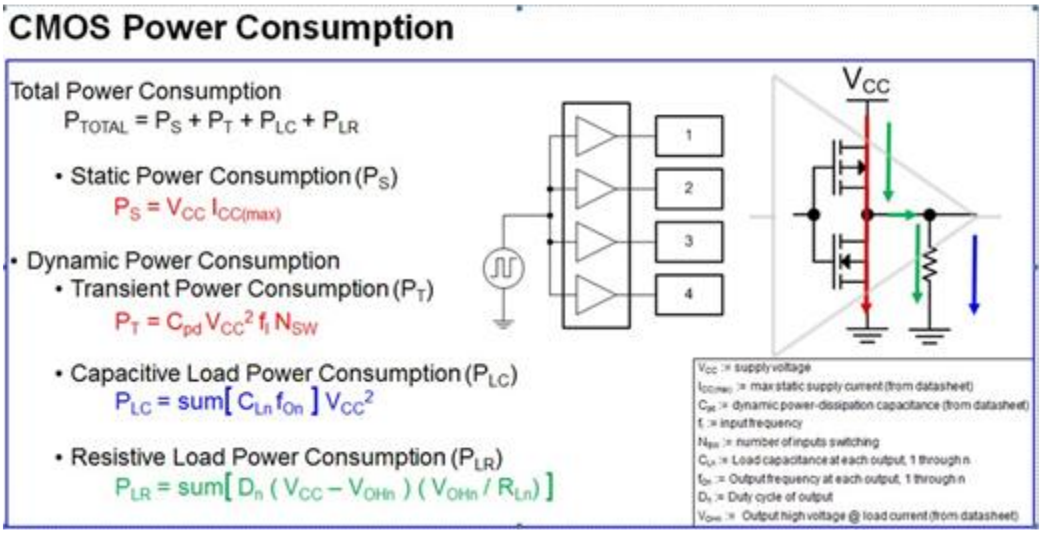


Fig. 1: Comparison between traditional modeling and machine learning-based regression workflows.



CMOS Power Consumption

Total Power Consumption

$P_{TOTAL} = P_S + P_T + P_{LC} + P_{LR}$

- Static Power Consumption (P_S)

  $P_S = V_{CC}\, I_{CC(max)}$

- Dynamic Power Consumption
  - Transient Power Consumption (P_T)

    $P_T = C_{pd} V_{CC}^2 f_I N_{SW}$

  - Capacitive Load Power Consumption (P_{LC})

    $P_{LC} = \text{sum}[\, C_{Ln} f_{On} \,] V_{CC}^2$

  - Resistive Load Power Consumption (P_{LR})

    $P_{LR} = \text{sum}[\, D_n (V_{CC} - V_{OHn}) (V_{OHn} / R_{Ln}) \,]$

V_{CC} := supply voltage
$I_{CC(max)}$:= max static supply current (from datasheet)
C_{pd} := dynamic power-dissipation capacitance (from datasheet)
f_I := input frequency
N_{SW} := number of inputs switching
C_{Ln} := Load capacitance at each output, 1 through n
f_{On} := Output frequency at each output, 1 through n
D_n := Duty cycle of output
V_{OHn} := Output high voltage @ load current (from datasheet)

Fig. 2: Limitations of traditional analytical and simulation-based power estimation methods.

Data-driven modeling approaches that can directly learn intricate nonlinear connections from empiri- cal data have been made possible by recent developments in machine learning. In contrast to conventional methods, machine learning models identify patterns from training data and generalize across unknown configurations rather than relying on explicit analytical equations. Because of this capacity, machine learning is especially well suited for power consumption prediction[5], where a number of circuit factors interact in a highly nonlinear way. Previous research has shown how well supervised learning approaches predict power and performance characteristics in digital circuits with lower estimate complexity [6, 7].

Figure 3 presents a conceptual overview of the proposed machine learning–based power prediction framework, illustrating the transformation of circuit-level parameters into predicted power values through supervised regression models.

Inspired by these findings, this research suggests a machine learning-based methodology that uses readily available circuit-level information to forecast the dynamic power consumption of logic circuits. Using logic-level power modeling, switching activity, load capacitance, supply voltage, operation fre- quency, and gate count are systematically varied to create a synthetic dataset. The capacity of many

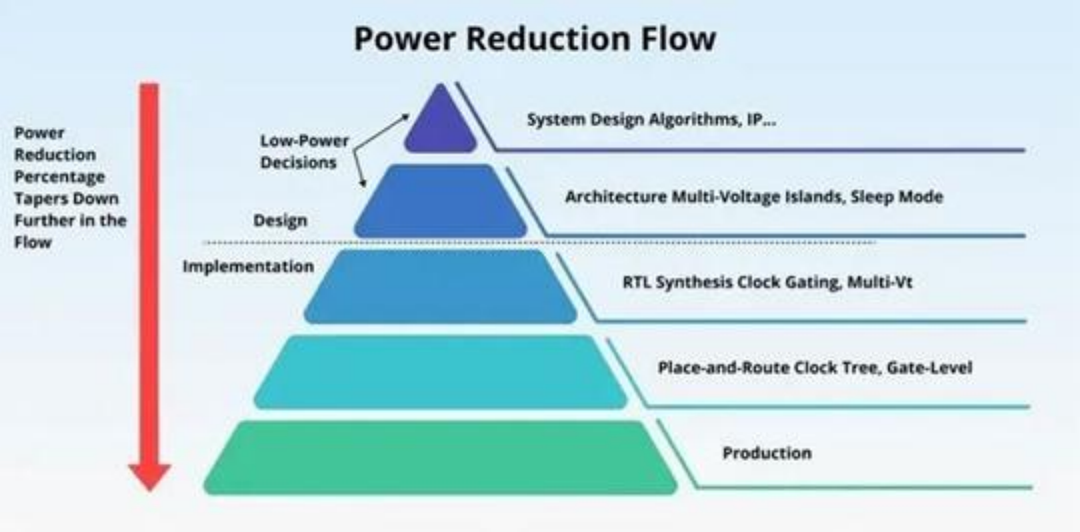


Fig. 3: Conceptual machine learning framework for logic circuit power prediction.

Supervised regression models to precisely and effectively represent nonlinear power behavior is assessed through training and evaluation. The creation of a repeatable synthetic dataset for logic circuit power modeling, the application and comparative assessment of several machine learning regression models for power prediction, and a thorough examination of prediction accuracy using conventional evaluation metrics are the main contributions of this work.

The suggested method facilitates early-stage power-aware design of logic circuits and offers a scalable and computationally efficient substitute for traditional power estimate techniques[8]. The rest of this work is structured as follows[9]. Related work is reviewed in Section II, the suggested technique is described in Section III, the implementation is described in Section IV, findings and discussion are presented in Section V, and future research directions are discussed in Section VI.

In contrast to many existing machine learning-based power estimation approaches that rely on post- layout data or technology-specific parameters, this work focuses on early-stage power prediction using only readily available circuit-level characteristics. This makes the proposed framework suitable for rapid design space exploration and technology-independent applications.

RELATED WORK

Because power consumption directly affects performance, dependability, and energy efficiency, it has long been a key area of study in digital and VLSI system design. Power consumption was evaluated using simple mathematical equations derived from switching activity, capacitive loading, supply voltage, and operating frequency in early studies that mainly concentrated on analytical power modeling methodolo- gies. Although these models were popular in the early phases of design and allowed for quick estimation, their inability to adequately depict complicated switching behavior in large-scale logic circuits was due to their idealized assumptions [3, 2]. Simulation-based power estimate techniques were developed to ad- dress the shortcomings of purely analytical approaches. By simulating real switching events and signal transitions, gate-level and transistor-level simulations provide in-depth understanding of circuit behavior. Vector-based analytical methods and probabilistic simulation greatly increased estimation accuracy and were adopted as standard procedures in electronic design automation processes [4]. Despite their accu- racy, these techniques are not suitable for quick design exploration because of their high computational cost and lengthy simulation timeframes, especially when used to contemporary circuits with millions of gates.

Power consumption estimation has long been a critical concern in digital and VLSI design because it directly affects energy efficiency, thermal stability, and system reliability. Early research primarily relied on analytical and simulation-based techniques derived from switching activity, capacitance, voltage, and frequency relationships [3, 4]. While these approaches provide reasonable accuracy, they often require detailed circuit information and incur significant computational overhead, especially for large-scale de- signs. As circuit complexity increases, the limitations of traditional estimation techniques become more pronounced, motivating the search for faster and more scalable solutions.

Recent advancements have introduced machine learning (ML) as a promising alternative for early-stage power estimation. ML-based approaches can learn nonlinear relationships directly from data without re- quiring exhaustive simulations. Studies such as [6, 7] demonstrate that regression and ensemble learning models can predict power metrics with reduced computational cost compared to simulation-driven meth- ods. These works highlight the capability of ML models to generalize across design configurations while maintaining acceptable accuracy levels.

The integration of ML into electronic design automation (EDA) has further expanded the scope of predictive modeling in circuit design. Surveys like [10] emphasize that ML techniques are increasingly used for estimating timing, area, and power across multiple design stages. More specialized works [11, 12] apply supervised learning to CMOS and digital circuit power estimation, reporting faster prediction times and competitive accuracy. However, many of these methods rely on post-layout data or technology-dependent parameters, limiting their applicability during early design exploration.

Recent research trends focus on lightweight and interpretable ML models that balance accuracy and computational efficiency. For instance, [**?**, 13, 14] show that ensemble and hybrid learning techniques can improve prediction robustness while using readily available circuit-level features. Despite these advance- ments, there remains a need for technology-neutral frameworks that support rapid early-stage design decisions. The present study addresses this gap by proposing a supervised learning framework that leverages simple circuit-level parameters for scalable and efficient power prediction.

Hybrid power estimation techniques that incorporated analytical models with sparse simulation data were investigated in later studies. These techniques used simulation-derived parameters to calibrate ana- lytical models in an effort to strike a compromise between computing efficiency and accuracy. Although hybrid approaches decreased simulation overhead, their generalization ability across various logic designs was frequently restricted, and their performance remained sensitive to circuit topology and operating circumstances.[15].

Researchers looked at statistical and probabilistic power estimation methods to deal with uncertainty and unpredictability in switching activity as semiconductor technology grew. Faster estimation for large circuits was made possible by these methods, which characterized signal transitions using probabilistic distributions instead of explicit input vectors. However, the accuracy of probabilistic approaches for large logic networks was diminished since they frequently needed assumptions regarding switching correlation and signal independence [16].

Power estimation problems in digital circuits now have more options thanks to the development of machine learning in recent years. Without using predetermined analytical equations, machine learning models may directly learn nonlinear correlations from data. Early research showed that power con- sumption and performance indicators in digital systems may be predicted using regression-based learning approaches with better accuracy than with conventional analytical models [6]. To improve prediction robustness and capture intricate parameter interactions, subsequent developments included ensemble learning techniques like Random Forests and Gradient Boosting. When it came to managing nonlin- ear relationships between circuit parameters, these models performed better, especially when operating circumstances changed [7]. However, a lot of these methods relied on post-layout characteristics or technology-dependent information, which limited their use in the early stages of design.

Additionally, deep learning-based power estimate techniques that use neural networks to simulate extremely complicated circuit behavior have been investigated. Deep learning techniques showed en- couraging accuracy, but they frequently needed big datasets, a lot of training time, and meticulous hyperparameter tweaking, which might be unfeasible for early-stage power analysis [17]. Furthermore, design insight and optimization are hampered by deep models' lack of interpretability.

Lightweight machine learning models that strike a compromise between computing economy and accuracy have been the focus of more recent research. These methods concentrate on utilizing readily available circuit-level characteristics, including switching activity and gate count, to enable quick power calculation in the absence of comprehensive designs data [18]. For early design exploration, when precise physical characteristics might not yet be accessible, these techniques are especially appropriate.

In conclusion, there are trade-offs between accuracy, computational cost, and generalization ability in current power estimating methods. For complicated designs, analytical models are inaccurate, simulation- based approaches are computationally expensive, and certain machine learning techniques rely on post- layout or technology-specific data. The creation of a generic, data-driven power prediction framework that facilitates early-stage logic circuit design and makes use of straightforward circuit-level parameters is motivated by these constraints. In order to close this gap, the current study suggests a supervised machine learning-based method that maintains computational efficiency and scalability while achieving accurate power prediction.

Recent trends in AI-driven electronic design automation also highlight the increasing role of machine learning in early design optimization. However, many existing solutions prioritize accuracy at the expense of interpretability or require large technology-dependent datasets. Therefore, lightweight and technology- neutral models remain an active research need.

METHODOLOGY

The suggested machine learning-based approach for forecasting the dynamic power consumption of logic circuits is presented in this section. The methodology's goal is to retain computational efficiency and scalability while enabling precise power prediction at early design phases utilizing readily available circuit- level characteristics. Fig. 4 shows the overall workflow of the suggested strategy, which includes feature selection and power modeling, dataset production, machine learning model building, and training and validation processes.

Power Modeling and Feature Selection

Signal switching activity and capacitive loading are the main factors that control dynamic power con- sumption in logic circuits. The following is a commonly used logic-level estimate of dynamic power consumption:

$$P = \alpha \cdot C_L \cdot V^2 \cdot f \qquad (1)$$

where f is the operating frequency, V is the supply voltage, C_L is the effective load capacitance, and α is the switching activity factor. Power consumption increases with circuit size in logic circuits made up of many gates. In order to represent structural complexity, gate count is included as an extra characteristic. Five circuit-level characteristics—switching activity, load capacitance, supply voltage, operating fre- quency, and gate count—are chosen as inputs to the machine learning models based on this formulation. These characteristics were selected because they are easily accessible in the early stages of design and because they together account for the majority of dynamic power dissipation. The average dynamic power consumption of the logic circuit is the goal variable for prediction.

Dataset Generation Strategy

To represent a variety of logic circuit designs and operating situations, a synthetic dataset is created. The chosen input attributes are systematically varied within reasonable and realistically applicable ranges during the dataset development procedure. Switching activity levels are altered to mimic variable signal transition probabilities, while load capacitance, supply voltage, and operation frequency adjusted to reflect operating state variations. Different logic circuit sizes are reflected by varying the gate count. The logic-level power model previously discussed is used to calculate the associated power consumption for each feature combination. A repeatable dataset that captures nonlinear correlations between circuit characteristics and power consumption may be created using this controlled dataset production technique. The final dataset is tabulated and utilized for the training and assessment of supervised machine learning models.

While synthetic data enables controlled experimentation and reproducibility, it may not capture all real-world parasitic and process variations. This limitation is acknowledged and motivates future validation using real EDA benchmark datasets.

Machine Learning Model Development

Learning a mapping between circuit-level variables and power consumption values is the aim of the su- pervised regression task used to design the power consumption prediction issue. The appropriateness of multiple regression models for capturing both linear and nonlinear relationships among input character- istics is assessed.

Because of its ease of use and interpretability, linear regression is utilized as a baseline model. Sup- port Vector Regression is chosen because it can use kernel functions to represent nonlinear interactions. Several decision trees are combined in Random Forest Regression, an ensemble learning technique that captures intricate feature interactions and enhances generalization performance. A thorough evaluation of prediction accuracy and resilience is made possible by the use of several regression models.

Training and Validation Procedure

To evaluate the model's capacity for generalization, the produced dataset is split into training and testing subsets. When necessary, feature scaling is used to guarantee steady learning and model convergence. The training dataset is used to train each machine learning model, which is then assessed using test data that has not yet been seen.

Standard regression evaluation metrics, such as Mean Absolute Error (MAE), Root Mean Square Error (RMSE), and coefficient of determination (R^2), are used to evaluate the model's performance. These measures offer complementary information on quality of fit, error size, and prediction accuracy. To improve robustness and lessen the effects of data partitioning bias, cross-validation is used.

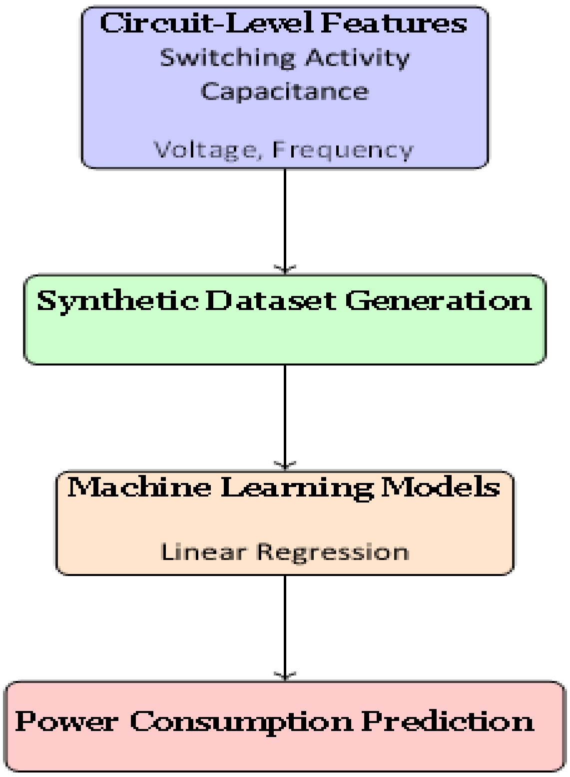


Fig. 4: Proposed machine learning–based methodology for logic circuit power consumption prediction.

IMPLEMENTATION

The suggested machine learning-based approach for forecasting power consumption in logic circuits is fully implemented in this part. By clearly outlining dataset preparation, preprocessing stages, model implementation, and assessment procedures, this section aims to guarantee experimental transparency and repeatability.

The implementation was done in a controlled offline environment that is appropriate for experimenting with machine learning and numerical computing. Dataset loading, feature preprocessing, supervised model training, prediction, and performance assessment make up the entire procedure. To establish a fair comparison between the implemented regression models, all experiments were carried out under the same conditions.

Dataset Preparation

The technique outlined in Section III was followed in the synthetic generation of the dataset utilized in this investigation. By methodically changing circuit-level factors that affect dynamic power usage, a variety of logic circuit designs are represented. Multiple input characteristics and the corresponding power consumption value are included in each data instance, which corresponds to a distinct logic circuit design.

Table I: Summary of the dataset used for experimentation

Attribute	Description
Dataset type	Synthetic, logic-level
Number of samples	5000 Number of input features 5
Target variable	Dynamic power consumption
Data format	Tabular (CSV)

The main features of the dataset utilized for testing are summarized in Table I.

The selected input features include switching activity, load capacitance, supply voltage, operating frequency, and gate count. These features are available during early design stages and capture the dominant contributors to dynamic power dissipation.

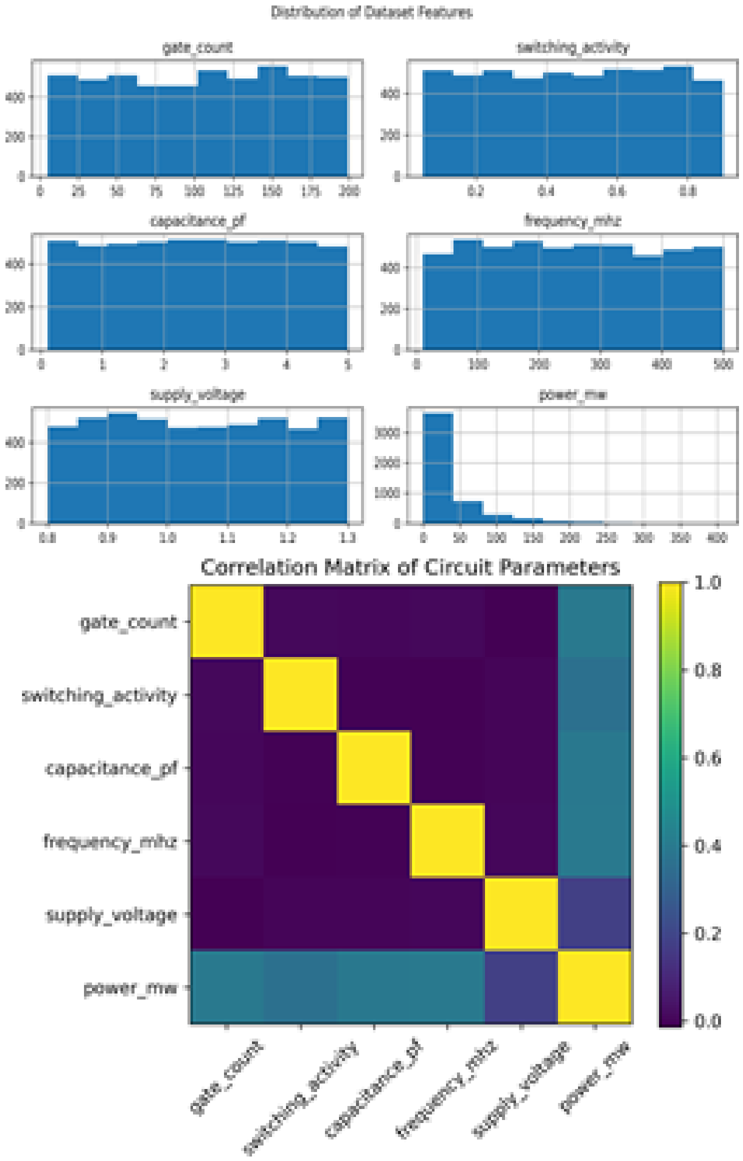


Fig. 5: Visualization of dataset characteristics: (left) distribution of input features and (right) correlation among circuit-level parameters.

Feature Preprocessing

Prior to model training, feature preprocessing was performed to improve numerical stability and learning behavior. Continuous-valued features were normalized to prevent bias toward parameters with larger numeric ranges. This step is particularly important for kernel-based regression models and contributes to consistent convergence during training.

Model Realization

To assess how well three supervised regression models predicted the power consumption of logic circuits. As a baseline model, linear regression was used to determine reference performance. To identify non- linear relationships between circuit characteristics and power usage, support vector regression was used. An ensemble-based method that can describe intricate relationships between input characteristics and increase prediction robustness is Random Forest Regression.

A summary of the machine learning models that have been implemented is shown in Table II.

Table II: Implemented machine learning models

Model	Description
Linear Regression	Linear baseline regression model
Support Vector Regression	Nonlinear regression using kernel methods
Random Forest Regression	Ensemble-based nonlinear regression model

To guarantee an objective evaluation of prediction performance, each model was trained using the training subset and tested on test data that had not yet been viewed.

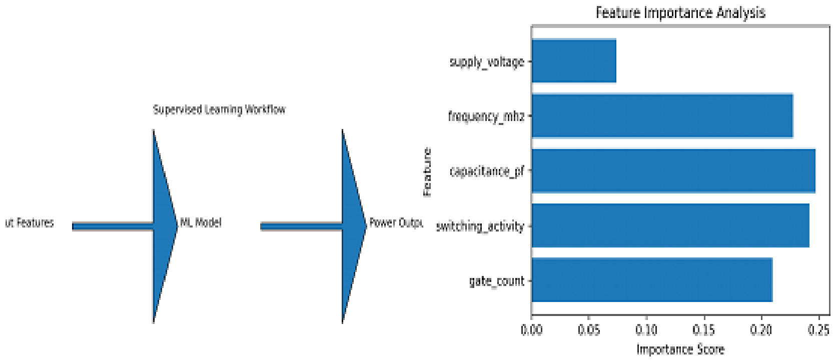


Fig. 6: Model realization and interpretability analysis: (left) supervised learning workflow and (right) feature importance derived from the ensemble model.

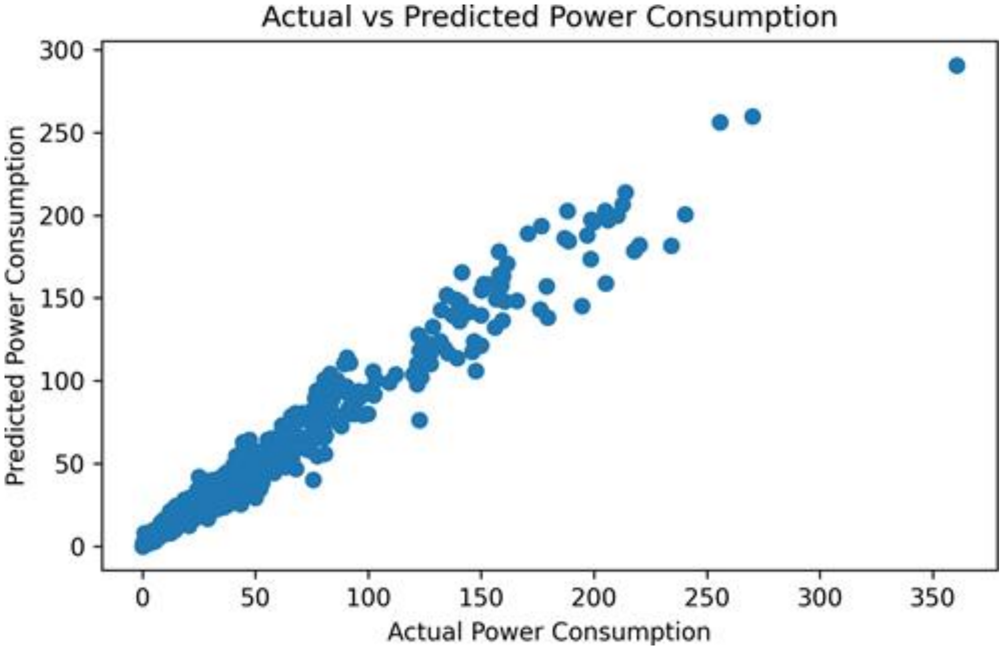


Fig. 7: Comparison between actual and predicted power consumption values obtained from the trained regression model.

Evaluation Process

Standard regression measures, such as Mean Absolute Error (MAE), Root Mean Square Error (RMSE), and coefficient of determination (R^2), were used to assess the model's performance. These measures allow for the objective evaluation of various models by offering complimentary insights into prediction accuracy, error size, and goodness of fit.

Future research may easily extend the suggested framework to other machine learning models or circuit parameters thanks to the structured implementation strategy, which guarantees repeatability.

RESULTS AND DISCUSSION

This part offers a thorough analysis of the observed performance as well as the experimental findings acquired utilizing the suggested machine learning-based power consumption prediction methodology. The goal is to assess how well various regression models forecast the power consumption of logic circuits and to examine how circuit-level characteristics affect prediction accuracy.

Evaluation of Model Performance

Mean Absolute Error (MAE), Root Mean Square Error (RMSE), and coefficient of determination (R^2) were used to assess the prediction performance of the built regression models. The average prediction error, error dispersion, and quality of fit between expected and actual power consumption numbers are all shown by these measurements taken together.

The quantitative performance of the assessed models is summarized in Table III.

Table III: Performance comparison of machine learning models

Model	MAE	RMSE	R^2
Linear Regression	20.2905	27.8204	0.6241
Support Vector Regression	5.2689	15.0652	0.8898
Random Forest Regression	4.2285	7.7417	0.9709

The Linear Regression model exhibits relatively high prediction error and a low coefficient of determi- nation, indicating its limited ability to capture the nonlinear relationship between circuit-level parameters and power consumption. This outcome is expected, as linear models are constrained by their assumption of linear dependency among features.

Support Vector Regression demonstrates a significant improvement in prediction accuracy compared to Linear Regression. The reduction in MAE and RMSE, along with an R^2 value close to 0.89, indicates that kernel-based regression is capable of modeling nonlinear dependencies more effectively. However, the performance of Support Vector Regression remains sensitive to feature scaling and kernel configuration. The Random Forest Regression model achieves the best performance across all evaluation metrics, with the lowest MAE and RMSE values and a high R^2 value of 0.9709. This result highlights the effectiveness of ensemble-based learning in capturing complex feature interactions and nonlinear power behavior. The aggregation of multiple decision trees enables robust prediction and improved generalization, particularly for datasets exhibiting nonlinear characteristics.

Visual Performance Analysis

Figure 8 presents a comparative visualization of the RMSE values obtained for different machine learn- ing models. The clear reduction in RMSE for the Random Forest model further confirms its superior prediction capability.

In addition, the agreement between predicted and actual power consumption values is illustrated through the scatter plot of actual versus predicted values. The strong clustering of data points along the diagonal line indicates high prediction accuracy and minimal systematic error, particularly for the ensemble-based model.

Feature Importance Analysis

To further analyze the contribution of individual circuit-level parameters, feature importance analysis was performed using the Random Forest Regression model. The results indicate that switching activity and operating frequency are the most influential factors affecting power consumption, which aligns with established dynamic power modeling theory. Load capacitance and supply voltage also contribute sig- nificantly, reflecting their direct involvement in dynamic power dissipation. Gate count captures circuit complexity and further enhances prediction accuracy by incorporating structural information.

Discussion and Implications

The experimental findings unequivocally show that employing a small number of circuit-level characteris- tics, machine learning models can accurately forecast logic circuit power usage. Because ensemble-based approaches can capture nonlinear connections and feature interactions, they perform better than both linear and kernel-based models. The suggested framework is especially appropriate for early-stage power- aware design and optimization as it provides a scalable and computationally effective substitute for conventional analytical and simulation-based power estimating methods.

Overall, the findings demonstrate the potential of data-driven methods to facilitate quick design space exploration and decision-making in digital circuit design and confirm the viability of using supervised machine learning techniques to logic-level power estimates.

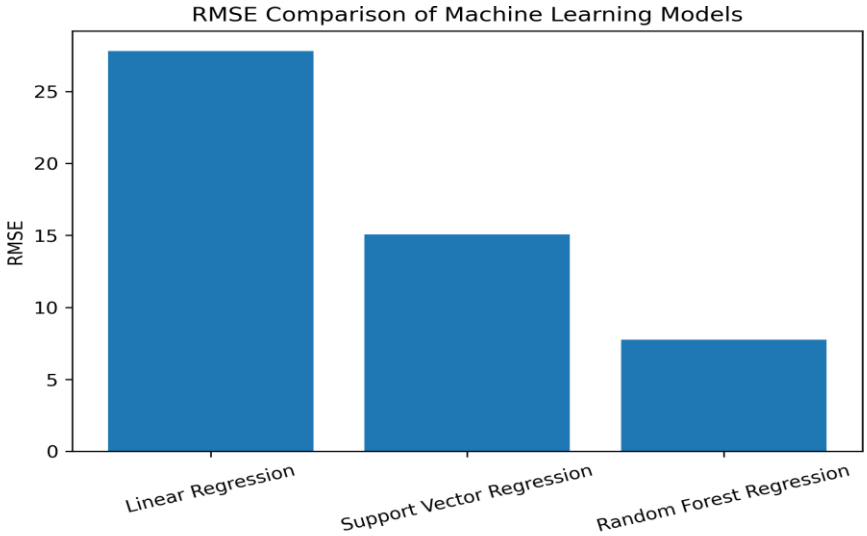


Fig. 8: Comparison of prediction performance of machine learning models using RMSE.

Computational Efficiency

Compared to simulation-based power estimation techniques that may require extensive runtime, the proposed machine learning models provide near-instantaneous inference once trained. Linear Regression has the lowest training complexity but limited accuracy, while Random Forest requires higher training time but offers fast inference and superior prediction performance. This trade-off makes ensemble learning practical for early-stage design exploration.

CONCLUSION

A machine learning-based methodology for forecasting logic circuit dynamic power consumption utilizing circuit-level characteristics was given in this article. By using supervised learning models to capture nonlinear interactions among important power-influencing parameters, the suggested method overcomes the drawbacks of traditional analytical and simulation-based power estimating methodologies. Logic-level power modeling was used to create a synthetic dataset that represented a variety of circuit designs and operating situations, allowing for controlled and repeatable testing.

Machine learning models can accurately and efficiently predict the power consumption of logic circuits, according to experimental assessment. With a mean absolute error of 4.2285, a root mean square error of 7.7417, and a coefficient of determination of 0.9709, Random Forest Regression outperformed the other models that were assessed. These findings demonstrate how ensemble-based learning approaches outperform linear and kernel-based models in simulating intricate feature interactions and nonlinear power dynamics.

The investigation also showed that the most important factors influencing power consumption are operating frequency and switching activity, which are followed by gate count, supply voltage, and load capacitance. This finding supports the use of circuit-level characteristics in the suggested framework and is in line with accepted dynamic power dissipation theories. Data-driven models are appropriate for early-stage power estimate, as evidenced by the high degree of agreement between anticipated and actual power levels. All things considered, the suggested framework provides a scalable, computationally effective, and technology-neutral approach to logic circuit power prediction. The method facilitates quick design space exploration and power-conscious decision-making in the early phases of digital system

design by depending on readily available circuit-level characteristics. Future research will concentrate on adding leakage power components, expanding the framework to sequential circuits, and assessing model performance across various technology nodes and real-world circuit benchmarks.

The proposed approach demonstrates the growing potential of data-driven techniques in modern electronic design automation and low-power VLSI design..

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